

Exhibit 2

U.S. Patent No. 8,549,339 (“’339 Patent”)**Accused Products**

Apple’s products comprising two or more sets of processors supporting or based on the Firestorm and Icestorm architectures, and similar efficiency core, performance core architectures, including without limitation the Apple M Series System of Chip (Apple M1 series, Apple M2 series, Apple M3 series, Apple M4 series), and the Apple A Series System on Chip beginning with Apple A10(Apple A10 series, Apple A11 series, Apple A12 series, Apple A13 series, Apple A14 series, Apple A15 series, Apple A16 series, Apple A17 series, and Apple A18 series), and all variants and iterations thereof (collectively, “Accused Products”), infringe at least Claims 1, 5, 8, 9, 10, 14, and 21 of the ’339 Patent.

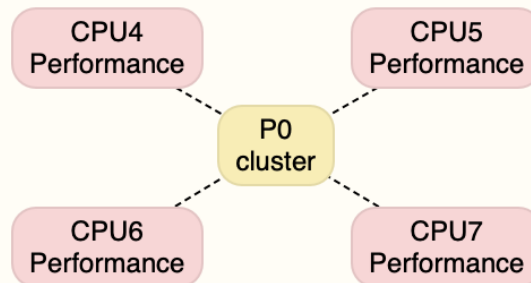
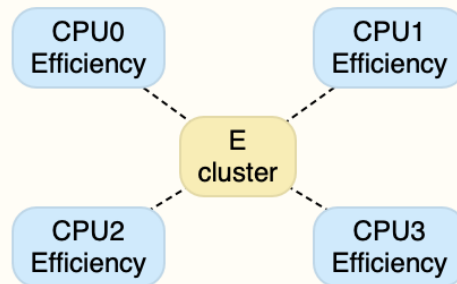
Each Accused Product infringes the claims in substantially the same way, and the evidence shown in this chart is similarly applicable to each Accused Product. For example, each Accused Product includes a Firestorm and Icestorm architectures or similar efficiency core, performance core architectures and, on information and belief, implements substantially the same architectural features described in the reference documentation cited in this chart. Thus, the descriptions and evidence below relating to the Apple M1 Series System on Chip representative products are similarly applicable to the remaining Accused Products listed above. Each claim limitation is literally infringed by each Accused Product. However, to the extent any claim limitation is not met literally, it is nonetheless met under the doctrine of equivalents because the differences between the claim limitation and each Accused Product would be insubstantial, and each Accused Product performs substantially the same function, in substantially the same way, to achieve the same result as the claimed invention. Notably, Defendant has not yet articulated which, if any, particular claim limitations it believes are not met by the Accused Products.

Claim 1

Claim 1	Accused Products
1. A multi-core processor, comprising:	<p>To the extent the preamble is limiting, each Accused Product comprises a multi-core processor.</p> <p>For example, the base model Apple M1 Series System on Chip contains eight cores implementing the Firestorm and Icestorm architecture. On information and belief other Accused Products provide a similar architecture with differing numbers of cores, for example the Max and Pro model Apple M Series System on Chip contain a greater number of cores implementing the Firestorm and Icestorm architecture.</p> <p><i>See, e.g.:</i></p>

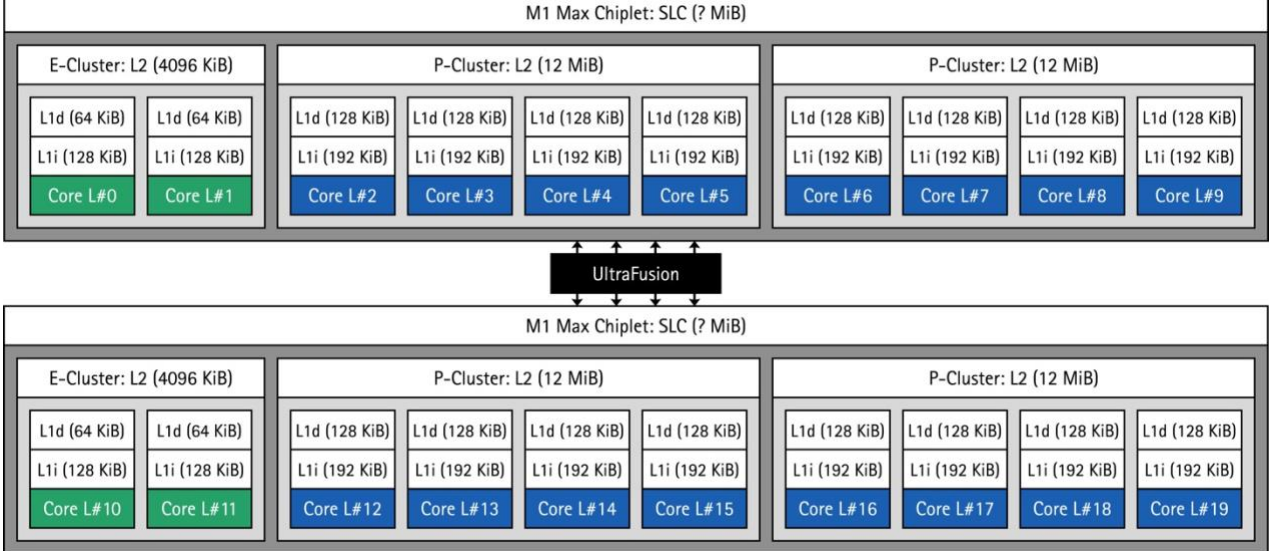
Claim 1	Accused Products
	<p>CPU</p> <p>At its heart, each M1 chip has a total of eight processor cores, all based on Apple's development of technology licensed from Arm. Four are described as Performance cores, dubbed <i>Firestorm</i>, and four are Efficiency cores, or <i>Icestorm</i>. These primarily differ in their compromise between performance and power consumption, with Firestorm cores performing in the same class as better Intel cores, and Icestorm delivering lower performance with much less power requirement and heat production. There are differences in the provision of cache memory, though:</p> <ul style="list-style-type: none"> • Firestorm has 192+128 KB L1 cache per core, and shares a total of 12 MB L2 cache. • Icestorm has 128+64 KB L1 cache per core, and shares a total of 4 MB L2 cache. <p>https://eclecticlight.co/2021/08/24/whats-in-an-m1-chip-and-what-does-it-do-differently/</p>

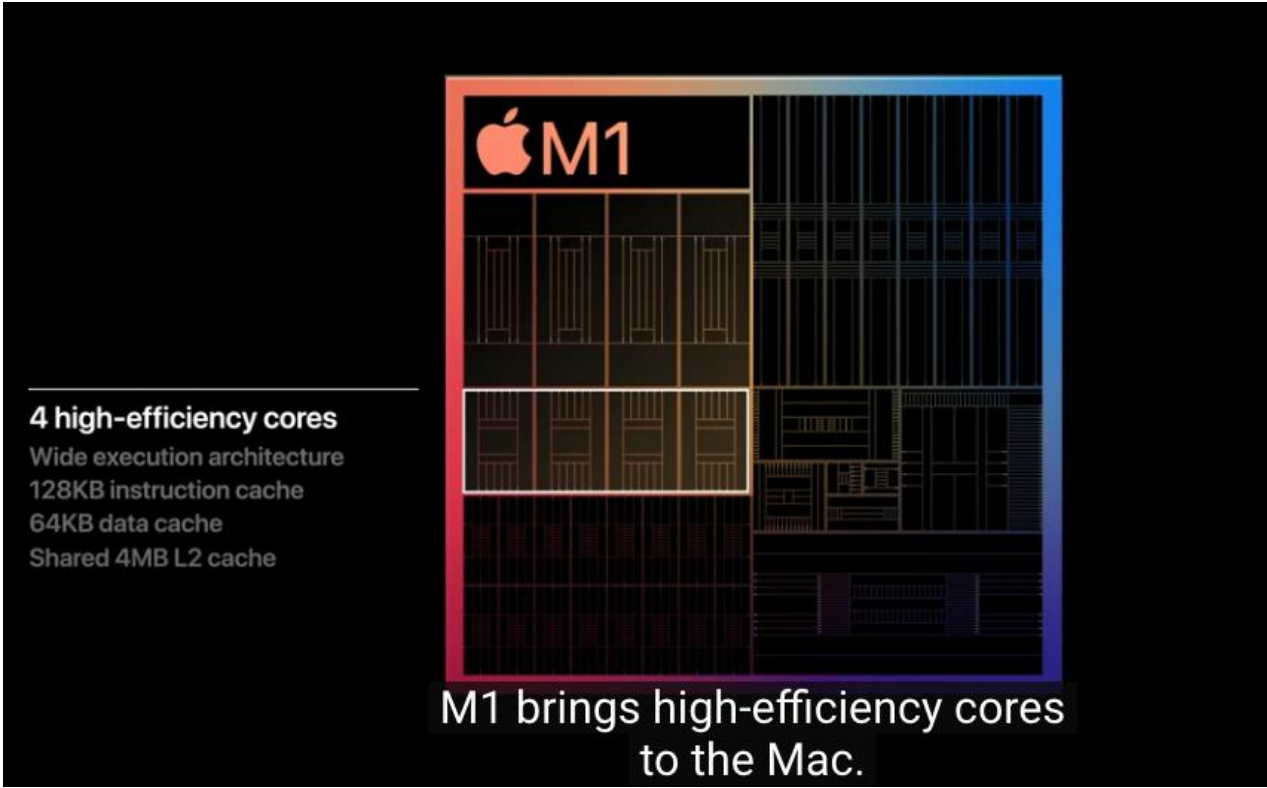
Apple M-series Chips: Base Model (M1-M3)



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<https://eclecticlight.co>

<https://eclecticlight.co/2024/02/19/apple-silicon-1-cores-clusters-and-performance/>

Claim 1	Accused Products
	 <p>The diagram illustrates the M1 Max chiplet architecture. It shows two identical chiplets, each labeled 'M1 Max Chiplet: SLC (? MiB)'. Each chiplet contains an 'E-Cluster: L2 (4096 KiB)' and two 'P-Cluster: L2 (12 MiB)'. The E-Cluster contains two cores (Core L#0 and Core L#1) with L1d (64 KiB) and L1i (128 KiB) caches. The P-Clusters each contain four cores (Core L#2 through Core L#5 for the first P-Cluster, and Core L#6 through Core L#9 for the second P-Cluster) with L1d (128 KiB) and L1i (192 KiB) caches. The two chiplets are connected via 'UltraFusion' technology. Below the diagram is a URL: https://www.sciencedirect.com/science/article/pii/S1383762124000390?ref=pdf_download&fr=R&R-2&rr=923601bc8d6a6c81#fig2</p>
<p>[1a] a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;</p>	<p>Each Accused Product comprises a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input.</p> <p>For example, the Apple M Series System on Chip contain a set of efficiency cores (e-cores) in an Icestorm architecture wherein each e-core from this set of e-cores is configured to receive a variable frequency depending on the computational load. To handle greater computational load with greater frequency, greater voltage is needed, so on information and belief, the set of e-cores is configures to receive a variable voltage, a first supply voltage. On information and belief the variable frequency is provided by a first PLL having a first clock signal as input. Identification of the precise mechanism used to provide a clock signal is proprietary information of Apple that is the proper subject of fact discovery.</p>

Claim 1	Accused Products
	<p><i>See, e.g.:</i></p> <div data-bbox="632 371 1892 1154">  <p>4 high-efficiency cores Wide execution architecture 128KB instruction cache 64KB data cache Shared 4MB L2 cache</p> <p>M1 brings high-efficiency cores to the Mac.</p> </div> <p>https://www.youtube.com/watch?v=5AwdkGKmZ0I at 9:02</p>


Claim 1	Accused Products
	<p>Variable frequency</p> <p>This is another key feature of Apple silicon cores: unlike most older CPUs, the cores can be run at different frequencies or clock speeds, ranging from 696 MHz up to 4,056 MHz for M3 P cores. Although I don't know whether M3 cores take advantage of this, it's also possible that their voltage is variable.</p> <p>Much of the time, E cores running background threads in an M3 chip do so with the cores at their minimum frequency of only 744 MHz, but when they're used to run threads that have overflowed from P cores their frequency can rise to their maximum of 2,748 MHz. Overflowed threads on E cores thus can't benefit from the same high performance as they would on P cores, but they do run much faster than background threads.</p> <p>Clusters</p> <p>Cores of the same type are grouped into clusters. Within each cluster, all the cores run at the same frequency, and they share local memory in their level 2 (L2) cache. That also makes it easier for threads to be moved around between cores in the same cluster. In M1 and M2 family chips, their E and P cores are arranged in clusters of up to four cores; Apple changed that in the M3, whose clusters can be of as many as 6 cores, all of the same type. In all base version CPUs of M-series chips, there's one cluster of 4 E cores, and one cluster of 4 P cores, so the CPU can be designated as being 4P+4E. Pro, Max and Ultra versions have different numbers of cores, and may have two (or more) clusters of P cores in all.</p> <p>https://eclecticlight.co/2024/02/19/apple-silicon-1-cores-clusters-and-performance/</p>

Claim 1	Accused Products
<p>[1b] a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and</p>	<p>Each Accused Product comprises a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal.</p> <p>For example, the Apple M Series System on Chip contain a set of performance cores (p-cores) in a Firestorm architecture wherein each p-core from this set of p-cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second phase lock loop (PLL) having a second clock signal as input.</p> <p>For example, the Apple M Series System on Chip contain a set of performance cores (p-cores) in a Firestorm architecture wherein each p-core from this set of p-cores is configured to receive a variable frequency depending on the computational load. To handle greater computational load with greater frequency, greater voltage is needed, so on information and belief, the set of p-cores is configured to receive a variable voltage, a second supply voltage. On information and belief the variable frequency is provided by a second PLL having a second clock signal as input. Identification of the precise mechanism used to provide a clock signal is proprietary information of Apple that is the proper subject of fact discovery. Additionally, the first supply voltage provided to the cluster of e-cores is independent from the second supply voltage provided to the cluster of p-cores and the first clock signal is independent from the second clock signal. For example, the e-cores and p-cores operate within different frequency ranges, requiring independent clock signals and supply voltages.</p> <p><i>See, e.g.:</i></p>

Claim 1	Accused Products
	<div data-bbox="632 264 1896 1109"></div> <p data-bbox="632 1133 1413 1174">https://www.youtube.com/watch?v=5AwdkGKmZ0I at 8:53.</p>

Claim 1	Accused Products
	<p>Variable frequency</p> <p>This is another key feature of Apple silicon cores: unlike most older CPUs, the cores can be run at different frequencies or clock speeds, ranging from 696 MHz up to 4,056 MHz for M3 P cores. Although I don't know whether M3 cores take advantage of this, it's also possible that their voltage is variable.</p> <p>Much of the time, E cores running background threads in an M3 chip do so with the cores at their minimum frequency of only 744 MHz, but when they're used to run threads that have overflowed from P cores their frequency can rise to their maximum of 2,748 MHz. Overflowed threads on E cores thus can't benefit from the same high performance as they would on P cores, but they do run much faster than background threads.</p> <p>Clusters</p> <p>Cores of the same type are grouped into clusters. Within each cluster, all the cores run at the same frequency, and they share local memory in their level 2 (L2) cache. That also makes it easier for threads to be moved around between cores in the same cluster. In M1 and M2 family chips, their E and P cores are arranged in clusters of up to four cores; Apple changed that in the M3, whose clusters can be of as many as 6 cores, all of the same type. In all base version CPUs of M-series chips, there's one cluster of 4 E cores, and one cluster of 4 P cores, so the CPU can be designated as being 4P+4E. Pro, Max and Ultra versions have different numbers of cores, and may have two (or more) clusters of P cores in all.</p> <p>https://eclecticlight.co/2024/02/19/apple-silicon-1-cores-clusters-and-performance/</p>

Claim 1	Accused Products
	<p>The World's Best CPU Performance per Watt</p> <p>M1 features an 8-core CPU consisting of four high-performance cores and four high-efficiency cores. Each of the high-performance cores provides industry-leading performance for single-threaded tasks, while running as efficiently as possible. They are the world's fastest CPU cores in low-power silicon, allowing photographers to edit high-resolution photos with lightning speed and developers to build apps nearly 3x faster than before. And all four can be used together for a huge boost in multithreaded performance.</p> <p>The four high-efficiency cores deliver outstanding performance at a tenth of the power. By themselves, these four cores deliver similar performance as the current-generation, dual-core MacBook Air at much lower power. They are the most efficient way to run lightweight, everyday tasks like checking email or browsing the web, and preserve battery life like never before. And all eight cores can work together to provide incredible compute power for the most demanding tasks and deliver the world's best CPU performance per watt.</p> <p>https://www.apple.com/newsroom/2020/11/apple-unleashes-m1/</p>
[1c] an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate	Each Accused Product comprises an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

Claim 1	Accused Products
<p>communication between the first set of processor cores and the second set of processor cores.</p>	<p>For example, the Apple M Series System on Chip include Apple's Unified Memory Architecture that is configured to facilitate communications between the e-cores and p-cores.</p> <p><i>See, e.g.:</i></p>  <p>https://www.youtube.com/watch?v=5AwdkGKmZ0I at 7:47</p>

Claim 1	Accused Products
	<div data-bbox="632 261 1898 1052"><div data-bbox="688 277 819 302">Framework</div><div data-bbox="688 329 888 378"><h2>Dispatch</h2></div><div data-bbox="688 399 1818 462"><p>Execute code concurrently on multicore hardware by submitting work to dispatch queues managed by the system.</p></div><div data-bbox="688 487 1575 506"><p>iOS 8.0+ iPadOS 8.0+ Mac Catalyst 13.0+ macOS 10.10+ tvOS 9.0+ visionOS 1.0+ watchOS 2.0+</p></div><div data-bbox="688 613 856 649"><h3>Overview</h3></div><div data-bbox="688 675 1797 760"><p>Dispatch, also known as Grand Central Dispatch (GCD), contains language features, runtime libraries, and system enhancements that provide systemic, comprehensive improvements to the support for concurrent code execution on multicore hardware in macOS, iOS, watchOS, and tvOS.</p></div><div data-bbox="688 784 1827 963"><p>The BSD subsystem, Core Foundation, and Cocoa APIs have all been extended to use these enhancements to help both the system and your application to run faster, more efficiently, and with improved responsiveness. Consider how difficult it is for a single application to use multiple cores effectively, let alone to do it on different computers with different numbers of computing cores or in an environment with multiple applications competing for those cores. GCD, operating at the system level, can better accommodate the needs of all running applications, matching them to the available system resources in a balanced fashion.</p></div><div data-bbox="632 1003 1308 1036"><p>https://developer.apple.com/documentation/Dispatch</p></div></div>

